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(Press release)

EFFECTIVE COMPRESSION OF QUANTUM BRAIDED CIRCUITS AIDED BY ZX-CALCULUS

Researchers at the National Institute of Informatics (NII) and Nippon Telegraph and Telephone Corporation (NTT) propose a new compression method to reduce the resources associated with large-scale fault-tolerant quantum circuits that brings practical quantum computation one step closer.

A major technical challenge for the realization of practical quantum computation comes from the very need for a large number of physical qubits to prevent errors from accumulating during that computation. The consequence of this is that a fault-tolerant quantum circuit for a given computation requires a huge amount of resources, both in terms of qubits and computational time. In this work published in Physical Review X on the 11th of November 2020, researchers have found an efficient method to compress such circuits with the purpose of decreasing their hardware demands. They use ZX-Calculus as an intermediate language to reduce both the number of qubits and time required to perform such computation in many different circuits. With their method they find an improvement of a 40% compression rate with respect to previous reductions, yielding compression rates higher than 70% compared to the initial circuit. The methodology proposed in this work promises to open new venues of research in large-scale quantum computing and bring quantum computation closer to reality by relaxing its hardware demands.

Background

The fast-paced development of quantum technology has brought quantum computing into the era of Noisy Intermediate-Scale Quantum (NISQ) devices, which have already served as the platform for early proof-of-principle experiments. However, they are still prone to errors which significantly accumulate during their operation. To realize a truly practical quantum advantage, the design of a fully operational large-scale quantum computer with high error tolerance is required. Current cutting-edge technology allows us to engineer NISQ devices with approximately 10^2 qubits, while fault-tolerant computers are expected to require millions of physical qubits at least to encode the logical information with sufficiently low error rates. This difference in size is currently the main obstacle for the development of large-scale fault-tolerant quantum computers.

We can expect that progress in hardware technology will bring scalability into quantum computer chip manufacturing and qubit controls in the future, however it is also possible for software to reduce the cost associated with fault-tolerant quantum computation implementations. Large-scale

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quantum computers will consist of many technological layers from the application level all the way down to the hardware, which will require various rounds of compilation and optimization. The resource cost will then come from the layers where quantum error correction codes are introduced to grant fault-tolerance for the implementation of the circuit. For most current quantum computer architectures, topological error correcting codes are the preferred ones, and in particular the surface code is expected to be used for superconducting-qubit based quantum computers where lattice-surgery or braiding is chosen for logical gate operation, the latter being more indicated for distributed quantum computation. A fault-tolerant implementation of quantum computational circuits not only makes the quantum computer larger, but also the runtime longer. “These operations require a high level of external control over quite an extended time. In turn this means the computation is more susceptible to errors”, Michael Hanks says. Therefore the possibility of compressing quantum circuits at the logical level not only implies a huge saving for the time and resources needed for quantum computation, but also lower errors. “Once a quantum algorithm or computation is compiled into a fault-tolerant circuit, to reduce both the amount of time and space required is paramount to bring practical quantum computers closer to reality”, says Marta Estarellas. Nonetheless, so far there is no established approach to tackle this problem and effective methods to treat these logical gate circuits have not been formulated.

Results

The researchers here propose an effective approach to the compression of braided fault-tolerant circuits on the 3D topological code. Braided circuits are generally represented as 3D structures, a low-level close-to-hardware language whose main elements are tubes or pipes that represent the defects or logical qubits. As shown in Figure 1, a quantum gate circuit can be represented as interlacing pipes, and is by manipulating these pipes that we can compress the quantum gate circuit. The main problem in the braided circuit reduction is that there are few and ad-hoc rules to manipulate these pipes. The first piece of this puzzle is to use ZX-calculus to do the compression, language that is equipped with a complete set of rules to manipulate logical gate circuits. However, we still need to solve another piece of the puzzle to harness ZX-calculus, and that is discovering the translation relations between ZX-calculus and the components of the braided circuit. The researchers have shown that these two representations of logical gate circuits can be mapped one to another by identifying a new interpretation hidden in ZX-calculus. After testing their new compression techniques against a set of test circuits they were able to reduce their volume by about 70% to the original volume in average.

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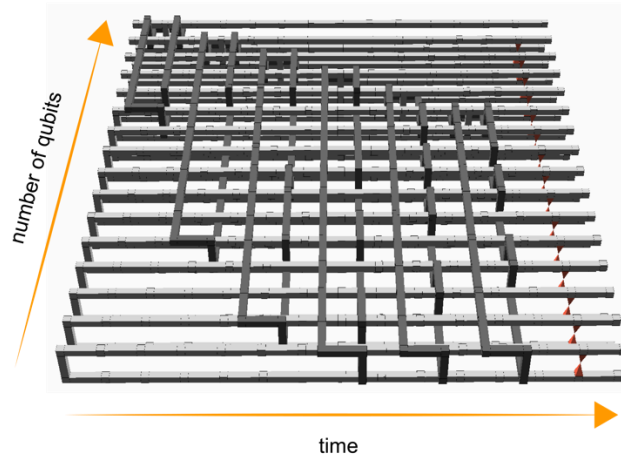


Figure 1 Illustrative example of a braided quantum circuit in the 3D representation.

The new approach also allows to unify the two main operations models used in surface-code based computation: lattice-surgery and braiding. “This unification promotes ZX-calculus from a representation of quantum logical circuits to a quantum computer language. We can now think about designing computer languages and compilers in the logical operation layer of the technological stack” says William J. Munro. Importantly, the unification of these two models also contributes directly to the compression. Taking the hybrid compilation approach, we can compress a circuit further, beyond what each individual approach had achieved.

Benchmarks		
Circuit	Vol_{init}	Vol_{opt}
Y-distillation	108	32 (-70.3%)
A-distillation	360	125 (-65%)
barenco-tof-3-after-light	510	262.125 (-48.6%)
mod-5-4-before	555	119.625 (-77.4%)
tof-4-before	882	420 (-52.4%)
vbe-adder-3-before	1995	563.5 (-72%)

Table 1 Computation volume and compression rates for a test suite of circuits used with this new method.

Methods

Previous approaches to fault-tolerant quantum circuit compression have suffered from the complexity of trying to reduce the circuits directly in the 3D representation. One of the key contributions of this new method is the inclusion of ZX-Calculus as an intermediate language to minimize the circuit volume. This diagrammatic language can be used to represent quantum processes and circuits in the form of tensor networks with a limited set of elements or nodes. That language can then apply a set of transformation rules (axioms) to change the structure of the network without modifying its underlying mathematical meaning (and hence its operation). We can apply these transformation rules carefully in such a way that the total number of nodes is reduced. As the set of transformations is complete, any minimal structure can be reached in principle. The compressed circuit

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in ZX-calculus is then mapped to the braided circuit by applying the newly identified relation between them.

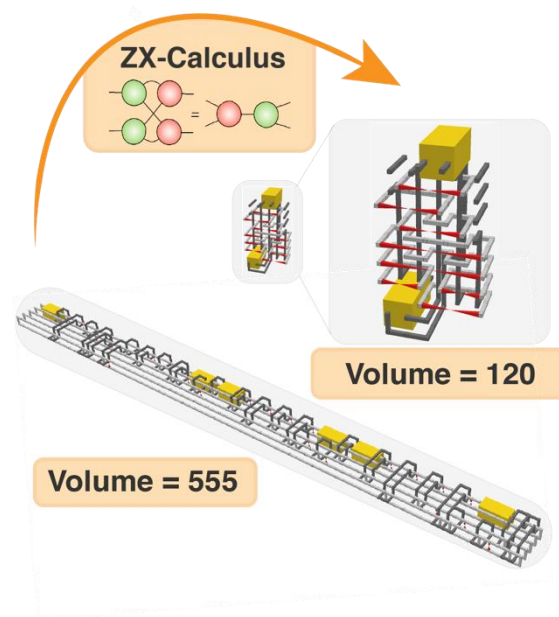


Figure 2 Compression of a quantum circuit with a 77.4% reduction rate.

Outlook

Global efforts are pushing quantum technology ahead rapidly with a steadily increasing number of qubits present in each next generation chip. Nevertheless, in the race to achieve practical quantum computing, it is not enough to just improve the hardware. Software techniques can significantly reduce the requirement for the quantum computer hardware, which can bring the realization of fault-tolerant quantum computer earlier by years. “The logical gate layer situates in the middle of the quantum computer technology stack, and our method can serve as a basis to further develop instruction set architectures and design quantum compilers” adds Kae Nemoto.

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